Remarks

In view of the foregoing amendments and following remarks responsive to the Final Office Action of September 28, 2006, Applicant respectfully requests favorable reconsideration of this application.

Allowed Subject Matter

Applicant respectfully thanks the Office for the indication claims 15, 18, 20, and 21 are allowed and that claims 7-14 are merely objected to.

Formal Matters

The Office objected to claim 10 under 35 U.S.C. §112, second paragraph, as being indefinite, asserting that the use of the term "third state" is unclear since the first and second states are not defined in claim.

While Applicant does not agree that this is a proper ground for objection to a rejection of the claim, Applicant has amended the language of claim 10 in such a manner as to make this rejection moot.

The Office also rejected claim 23 under 35 U.S.C. §112, second paragraph, asserting that the claim does not properly recite the structural cooperative relationships between the so-called circuitry components.

While Applicant disagrees that the claim form is deficient, the structural relationship between the various components being implicit, Applicant has amended the claim to more expressly recite the structural relationships between the circuitry components.

Prior Art Rejections

The Office rejected claims 1-3, 5, 6, 22, and 23 under 35 U.S.C. 103(a) as being unpatentable over Philips in view of the I2C specification. The Office asserted that Philips discloses all of the subject matter of the independent claims 1 and 23, except for the use of I2C extended addressing wherein a message comprises a command code

having a plurality of bits, a first subset of bits functioning as an indicator of the type of supplemental address.

However, the Office asserted that, the use of extended addressing is old and well-known, such as is illustrated by the 10 bit addressing of the I2C specification itself.

The Office asserted that, in the I2C 10 bit addressing scheme, when a 10 bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests if the 8th bit (R/W direction bit) is 0; it is possible that more than one device will find a match and generate an acknowledge (A1); and all slaves that found a match will compare the 8 bits of the second byte of the slave address with their own addresses, but only one slave will find a match and generate an acknowledge (A2). According to the Office, the message contains a first byte and a second byte; the first byte is 11110XX, where XX are the two MSBs of the 10 bit addressed slave and the second byte comprises the eight LSBs of the 10 bit addressed slave. The Office asserted that this first byte, including the two MSBs, serves as an indicator that the supplemental address is a 10 bit address and the second byte is readable on the so-called "supplemental address".

The Office asserted that, since both references are from the same field of endeavor, the purpose disclosed by the I2C specification would have been recognized in the pertinent art of Philips and, thus, it would have been obvious to provide Philips with the extended addressing scheme as taught by the I2C specification for the purpose of extending the number of devices that can be connected to the I2C bus.

Applicant respectfully traverses. The portion of Philips relied upon by the Office discloses the standard I2C addressing protocol described at page 1, line 26 through page 2, line 2 in the background section of the present application. The 10 bit addressing protocol of the I2C specification referenced by the Office also was discussed in the background section of the present application at page 2, lines 3-5. Accordingly, the two references relied upon by the Office do not appear to teach anything other than the I2C protocol that is expressly discussed in the background section of the present application.

Specifically, the proposed combination comprises the 10 bit addressing scheme of the I2C specification in combination with the internal addressing scheme of the I2C specification, as described on page 1, line 26 to page 2, line 5 of the present application.

This "combination" comprises a first byte after the start bit (comprising 11110XX, where XX represents the two MSBs of the slave address) followed by a read/write bit, followed by a second byte containing the lower eight bits of the 10 bit address, followed by a third byte containing an internal address in the slave device. It appears that, in the Office's analysis, the "11110" portion of the first byte corresponds to the "indicator bits" and the second byte corresponds to the internal address.

This "combination", however, does not correspond to the claimed addressing technique. Claim 1 recites that the "indicator bits" indicate the internal address. In the aforedescribed I2C scheme, (1) the 11110 bits indicate the addressing scheme for the external address of the slave device (particularly, that it is the 10 bit addressing scheme as opposed to the 7 bit addressing scheme), not the addressing scheme of the internal address inside the slave device and (2) the second byte is the external address of the slave device.

This is a different scheme than the claimed addressing technique. In the I2C "combination" described in the Office Action, (1) it is the third byte that indicates the internal address and (2) there is only one scheme for the internal address (i.e., it is an 8 bit address).

In short, the proposed combination (1) actually is not a "combination" at all since it is nothing more than a description of the I2C 10-bit addressing scheme with the first "data" byte (the third overall byte) used to indicate an internal register address, as described in the background section of the present application and (2) does not correspond to the claimed invention. Accordingly, the asserted prior art does not teach that for which it has been cited.

Turning specifically to the language of claim 1, the cited prior art does not teach "sending a message comprising a command code... comprising... a first subset of said bits functioning as an indicator of a type of the supplemental address that is being

provided", wherein the "slave device determine[s] an internal address for said slave device using said supplemental address".

Accordingly, the prior art does not teach the claimed addressing technique. It is respectfully submitted that Applicants' invention as recited in claim 1 is neither taught by nor obvious in view of the cited reference. Dependent claims 2, 3, 5, and 6, depend directly or indirectly from claim 1 and, therefore, are allowable for at least all of the reasons set forth above in connection with claim 1. Withdrawal of the rejection of claims 1-3, 5 and 6 is respectfully requested.

With reference to independent claims 22 and 23, the cited prior art does not teach "at least one indicator bit indicating the format of the internal address portion of the array" (claims 22 and 23) or "interpreting said at least one indicator bit to determine the format of said internal address" (claims 22 and 23) or "interpreting said internal address portions of said array in accordance with said determined format" (claims 22 and 23). . It is respectfully submitted that Applicants' invention, as recited in claims 22 and 23, is neither taught by nor obvious in view of the cited reference. Withdrawal of the rejection of claims 22 and 23 is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims remaining in this application are now in condition for allowance. Applicant respectfully requests the Office to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

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/Theodore Naccarella/
Theodore Naccarella,
Reg. No. 33,023
Synnestvedt & Lechner LLP
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107
Telephone: (215) 923-4466
Facsimile: (215) 923-218
Attorneys for Applicant